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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,035	05/07/2007	Zheng Shen	GWS-009	1665

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
02/18/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/582,035	SHEN ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-12,18 and 19* is/are allowed.

6)☒ Claim(s) *1,3,4,6,13-17 and 20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/12/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 25, 2008 has been entered.

Drawings

2. Figures 1A, 1B, and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 3, 4, 6, 13, 14, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli et al. (US 6,455,905 B1, prior art of record) in view of Mehta et al. (US 6,261,944 B1).

a. Regarding claim 1, **Perugupalli discloses a monolithic structure** (e.g. figure 11, and clarified in the figure below), **comprising:**

a first pair of devices (devices 1 and 2, as seen in the figure below) **and a second pair of devices** (devices 3 and 4, as seen in the figure below), **each pair of devices comprising:**

a first lateral device having a first source terminal, a first drain terminal, and a first gate terminal (e.g. first lateral devices 1 and 3 each have a source, drain, and gate terminal, and are lateral, as seen in the figure below and

clarified in figures 4, 6, and 9 of Perugupalli), **each of said first source, first drain, and first gate terminals terminating on a first surface of a semiconductor substrate** (e.g. as seen the figure below and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320), **and**

and a second lateral device having a second source terminal, a second drain terminal, and a second gate terminal (e.g. second lateral devices 2 and 4 each have a source, drain, and gate terminal, and are lateral, as seen in the figure below and clarified in figures 4, 6, and 9 of Perugupalli), **each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate** (e.g. as seen the figure below and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320), **and**

wherein (i) in each pair of devices, said first drain terminal is connected to said second drain terminal (e.g. as seen in the figure below, first drain terminal of device 1 is connected to second drain terminal of device 2 via the drain lead 143, and first drain terminal of device 3 is connected to second drain terminal of device 2 via the drain lead 144)**, and said first gate terminal is connected to second to said second gate terminal** (e.g. first gate terminal of device 1 is connected to second gate terminal of device 2 via gate lead 141, and first gate terminal of device 3 is connected to second gate terminal of device 4 via gate lead 142),

(ii) in each pair of devices, each first lateral device is combined with each second lateral device on said substrate (e.g. as seen in figure 11), **(ii) both first source terminals are connected to both second source terminals to define a common source terminal of the monolithic structure** (e.g. as seen in the figure, both first source terminals are connected to both second source terminals via common source terminal 124), **and**

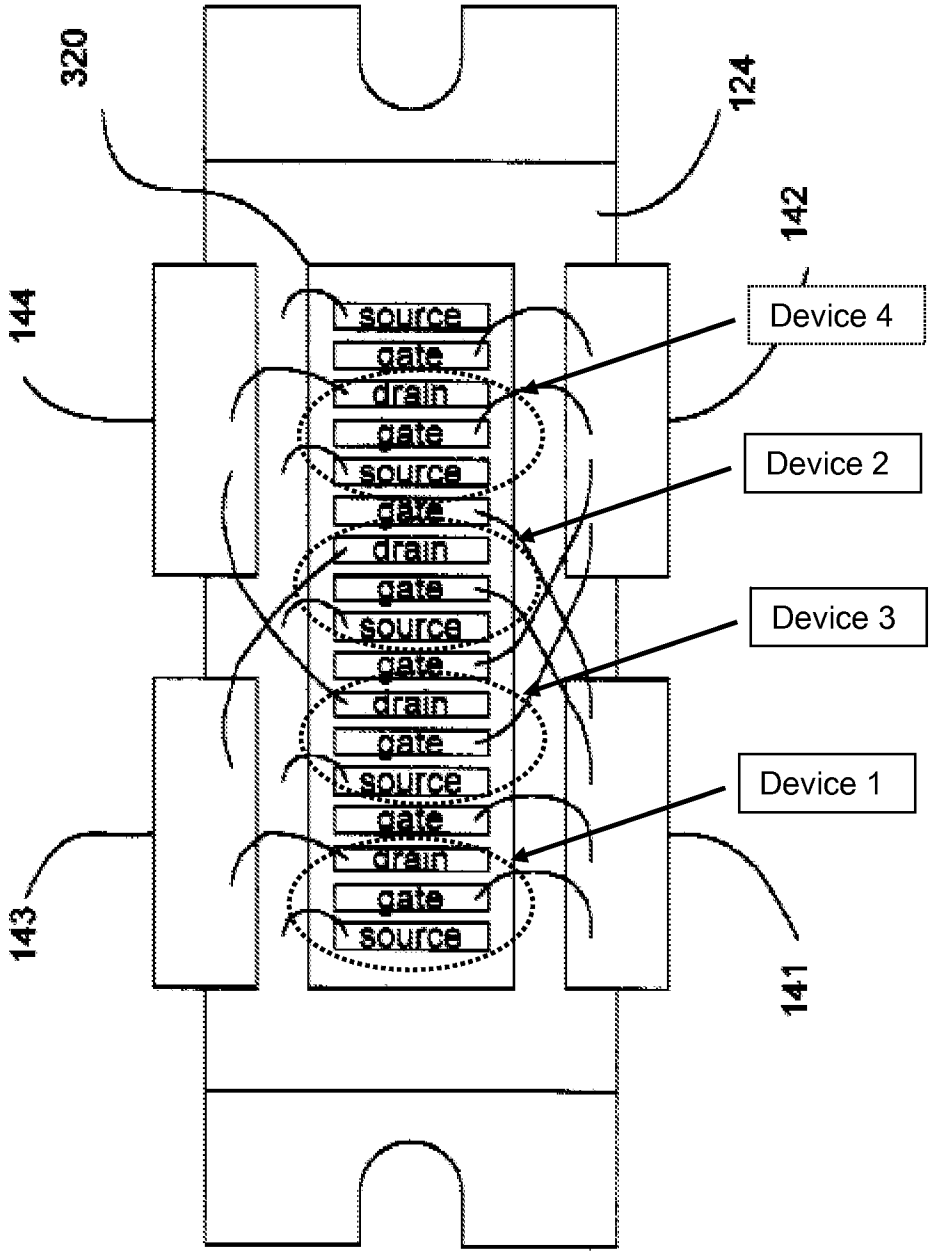
(iv) a first electrically isolated lead comprises the common source terminal (source terminals are connect to each other via wire bonding to the isolated lead 124, as seen in figure 11 and disclosed in col. 5, lines 14 – 19).

Perugupalli is silent with respect to a multi-layer metal interconnect structure disposed above each pair of devices, the connections between the drains, sources, and gates being made by the interconnect structure, and the multi-layer interconnect structure including the first electrically isolated lead comprising the source terminal.

Mehta discloses a monolithic structure (e.g. figure 5), **wherein a multi-layer interconnect structures is disposed over a plurality of devices** (interconnect structure 14 disposed over MOS transistors in device layer 12), **wherein the sources, drains, and gates of the devices may be connected** (e.g. as seen in the figure). **Furthermore, Mehta discloses an isolated lead may be included on the interconnect structure** (lead 6).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Perugupalli such that a multi-

layer interconnect structure was disposed over the substrate and devices, since Perugupalli discloses the devices to be formed monolithically in a semiconductor substrate (e.g. as seen in figure 09), with sources and drains connected in the claimed manner, and Mehta discloses that multi-layer interconnect structures may be disposed over monolithic device structure and used to connect the sources, drains, and gates of the devices . One would have been motivated to form a multi-layer interconnect structure over the devices of Perugupalli in order to create a device with less wire bonds, therefore more tolerant to external forces and less likely to have a broken lead that are associated with the thin wires of wire bonding.



b. Regarding claim 3, **Perugupalli in view of Mehta disclose the monolithic structure of claim 1, as cited above, wherein said first and second drain terminals of the first pair of devices are electrically**

independent of the first and second drain terminals of the second pair of devices (e.g. as seen in the figure above, first and second drain terminals of the first pair of devices, 1 and 2, are connected to drain lead 143, while first and second drain terminals of the second pair of devices, 3 and 4, are connected to drain lead 144. Therefore, they are independent).

c. Regarding claim 4, **Perugupalli in view of Mehta disclose the monolithic structure of claim 3, as cited above, wherein said first and second gate terminals of the first pair of devices are electrically independent of the first and second gate terminals of the second pair of devices** (e.g. as seen in the figure above, first and second gate terminals of the first pair of devices, 1 and 2, are connected to gate lead 141, while first and second gate terminals of the second pair of devices, 3 and 4, are connected to gate lead 142. Therefore, they are independent).

d. Regarding claim 6, **Perugupalli in view of Mehta disclose the monolithic structure of claim 1, wherein each of said first and second lateral devices comprises a lateral power MOSFET** (e.g. col. 3, line 60 discloses the transistors to be LDMOS transistors, and col. 1, lines 14 - 16 disclose that LDMOS (laterally diffused MOSFET) transistor may be used for power applications).

e. Regarding claim 13, **Perugupalli discloses a monolithic structure comprising at least for lateral power transistor devices combined on a semiconductor substrate** (e.g. figure 11, and clarified in the figure above), **said structure comprising:**

a first pair of power transistor devices (power transistor devices 1 and 2, as seen in the figure above) **and a second pair of power transistor devices** (power transistor devices 3 and 4, as seen in the figure above), **each pair of power transistor devices comprising:**

a first lateral power transistor device comprising a first source terminal, a first drain terminal, and a first gate terminal (e.g. first lateral devices 1 and 3 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320), **and**

a second lateral power transistor device having a second source terminal, a second drain terminal, and a second gate terminal (e.g. second lateral power transistor devices 2 and 4 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **said second source, second drain, and second gate terminals terminating on said first surface** (e.g. as seen the figure above and

clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320), **and**

wherein (i) in each pair of first and second devices, said first drain terminal is connected to said second drain terminal (e.g. as seen in the figure above, first drain terminal of device 1 is connected to second drain terminal of device 2 via the drain lead 143, and first drain terminal of device 3 is connected to second drain terminal of device 2 via the drain lead 144), **and said first gate terminal is connected to said second gate terminal** (e.g. first gate terminal of device 1 is connected to second gate terminal of device 2 via gate lead 141, and first gate terminal of device 3 is connected to second gate terminal of device 4 via gate lead 142),

(ii) said first and second gate terminals of the first pair of power transistor devices are electrically independent of the first and second gate terminals of the second pair of power transistor devices (e.g. as seen in the figure above, first and second gate terminals of the first pair of devices, 1 and 2, are connected to gate lead 141, while first and second gate terminals of the second pair of devices, 3 and 4, are connected to gate lead 142. Therefore, they are independent);

(iii) said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of devices (e.g. as seen in the figure above, first and second drain terminals of the first pair of devices, 1 and 2, are connected to drain lead 143,

while first and second drain terminals of the second pair of devices, 3 and 4, are connected to drain lead 144. Therefore, they are independent),

(iv) a first electrically isolated lead comprises both first source terminals connected to both second source terminals (e.g. as seen in the figure above, both first source terminals are connect to both second source terminals via common source terminal 124),

(v) a second electrically isolated lead comprises said first and second drain terminals of the second pair of power transistor devices (lead 143),

(vi) a third electrically isolated lead comprises said first and second drain terminals of the second pair of power transistor devices (lead 144);

(vii) a fourth electrically isolated lead comprises said first and second gate terminals of the first pair of power transistor devices (lead 141), **and**

(viii) a fifth electrically isolated lead comprising said first and second gate terminals of the second pair of power transistor devices (lead 142).

Perugupalli is silent with respect to a multi-layer metal interconnect structure disposed above each pair of devices, the connections between the drains, sources, and gates being made by the interconnect structure, and the multi-layer interconnect structure including the first, second, third, fourth, and fifth electrically isolated lead.

Mehta discloses a monolithic structure (e.g. figure 5), **wherein a multi-layer interconnect structures is disposed over a plurality of devices** (interconnect structure 14 disposed over MOS transistors in device layer 12), **wherein the sources, drains, and gates of the devices may be connected** (e.g. as seen in the figure). **Furthermore, Mehta discloses an isolated lead may be included on the interconnect structure** (lead 6).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Perugupalli such that a multi-layer interconnect structure was disposed over the substrate and devices, since Perugupalli discloses the devices to be formed monolithically in a semiconductor substrate (e.g. as seen in figure 09), with sources and drains connected in the claimed manner, and Mehta discloses that multi-layer interconnect structures may be disposed over monolithic device structure and used to connect the sources, drains, and gates of the devices . One would have been motivated to form a multi-layer interconnect structure over the devices of Perugupalli in order to create a device with less wire bonds, therefore more tolerant to external forces and less likely to have a broken lead that are associated with the thin wires of wire bonding.

f. Regarding claim 14, **Perugupalli in view of Mehta disclose the monolithic structure of claim 13, as cited above, wherein each of said first and second lateral power transistor devices comprises a lateral power**

MOSFET (e.g. col. 3, line 60 discloses the transistors to be LDMOS transistors, and col. 1, lines 14 - 16 disclose that LDMOS (laterally diffused MOSFET) transistors may be used for power applications).

g. Regarding claims 17 and 20, **Perugupalli in view of Mehta disclose the monolithic structure of claims 1 and 13, as cited above respectively, wherein each of the first and second lateral devices comprise source and drain dopants of a same type** (e.g. as seen in figure 09 of Perugupalli, the source and drain regions have the same drain dopant type, which is n-type. It is within the level of one of ordinary skill in the art to extend this doping scheme that that depicted in the other embodiments, such as the embodiment shown in figure 11. One would have been motivated to make the dopant scheme of figure 9 for that shown in figure 11 in order to create an n-type MOS device, comprising all n-type MOS transistors)

6. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli in view Mehta and Green.

a. Regarding claim 15, **Perugupalli in view of Mehta disclose the monolithic structure of claim 13, but is silent with respect to the size of said second lateral power transistor being smaller than a size of said first lateral power transistor.**

Green teaches that for multiple transistors on the same substrate, the size of the second transistor may be smaller than the size of the first transistor (col. 4, lines 59 - 61).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli in view of Mehta such that the second power transistor is smaller than the first, since it was known in the art to make transistors of different sizes in a monolithic structure, as disclosed by Green. One would be motivated to make such a modification since the electrical characteristics, such as the switching speed or current through the device can be affected by reducing dimension size.

b. Regarding claim 16, **Perugupalli in view of Mehta discloses the monolithic structure of claim 13, but is silent with respect to a first threshold voltage of said first lateral power transistor being different from a second threshold voltage of said second lateral power transistors and a difference in said first and second threshold voltages is at least ranging approximately 0.1 V.**

Green teaches that for multiple transistors on the same substrate the threshold voltages may be different by up to 1.75 V (e.g. table in col. 3).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli in view of Mehta such that the threshold voltages of the two power transistors of a

monolithic structure differ by over 0.1 V, since Green teaches that such modifications are known in the art. One would be motivated to make such a modification in order to allow for more flexibility in circuit design, as well as for an increase in transistor switching speed, as disclosed in Green (col. 3, lines 52 - 53, and col. 4, lines 33 - 34).

Allowable Subject Matter

7. **Claims 7 – 12, 18, and 19 are allowed.**

8. The following is a statement of reasons for the indication of allowable subject matter:

a. Regarding claim 7, the Applicant has argued that the combination of the prior art of Forbes is non-obvious and destroys the teachings of the primary reference of Perugupalli. In particular, the Applicant argues that the structure of Forbes requires transistors of opposite conductivity type, however the transistors of Perugupalli are all the same conductivity type, and therefore the combination of Forbes will destroy the device of Perugupalli. The Examiner finds the Applicant's arguments persuasive.

Claim 7 recites a monolithic device comprising 4 lateral power transistors, in which a first and second MOSFET is connected in parallel for form a first pair, and similar for a second pair, and the first pair is connected to the second pair via a multi-layer metal interconnect structure disposed on the monolithic structure. The lateral power transistors have a common source, and drain and gate

connections in a fashion to yield a self-driven synchronous rectification device. There is nothing in the prior art that anticipates or renders obvious such connections in a monolithic structure with lateral power transistors and a multi-layer interconnect structure to connect the terminals in the claimed invention.

Claims 8 and 18 depend on claim 7.

Regarding claim 9, the Applicant has argued that the combination of the prior art of Alder is non-obvious and destroys the teachings of the primary reference of Perugupalli. In particular, the Applicant argues that the structure of Perugupalli requires each pair of transistors to be separately connected and 180^{o} out of phase with the other pair of transistors, however the pairs of transistors of Alder are all connected and in-phase. Therefore the combination of Alder will destroy the device of Perugupalli. The Examiner finds the Applicant's arguments persuasive.

Claim 9 recites a monolithic device comprising 4 lateral power transistors, in which a first and second MOSFET is connected in parallel for form a first pair, and similar for a second pair, and the first pair is connected to the second pair via a multi-layer metal interconnect structure disposed on the monolithic structure. The lateral power transistors have a common source and common gate connections, and drain connections in a fashion to yield an externally driven synchronous rectification device. There is nothing in the prior art that anticipates or renders obvious such connections in a monolithic structure with lateral power

transistors and a multi-layer interconnect structure to connect the terminals in the claimed invention.

Claims 10, 11, 12 and 19 depend on claim 9.

9. **Claim 5** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. For similar reasons as cited above with respect to claim 7, claim 5 has allowable subject matter.

Response to Arguments

10. Applicant's arguments filed November 25, 2008 have been fully considered but they are not persuasive. With respect to the arguments directed towards the amendment "*a multi-layer metal interconnect structure*", the Applicant argues that it would have not have been obvious to one of ordinary skill in the art to employ a multi-layer interconnect structure in the device of Perugupalli. The Examiner respectfully disagrees. Although Perugupalli discloses wire-bond connections for the source, drain, and gate terminals, it is well-known in the art that connections between source, gate, and drain regions may be formed by multi-layer metal interconnect structures formed on the substrate surface, as supported by Mehta. Furthermore, the combination of the multi-layer metal interconnect structure would not destroy the intent purpose of the device of Perugupalli since the gate, source, and drain connections would still be maintained, and the device would remain operational. Furthermore, one would be

motivated to formed a multi-layer interconnect structure on the monolithic substrate of Perugupalli in order to eliminate the fragile wire-bonds formed, and create a more rigid structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 2892
February 12, 2009

/Lex Malsawma/
Primary Examiner, Art Unit 2892